Enrollment No: _____ Exam Seat No:_____

C.U.SHAH UNIVERSITY

Summer Examination-2017

Subject Name: Digital Circuits
Subject Code: 4TE03DCI1 Branch: B.Tech(Electrical)

Semester: 3 Date: 27/03/2017 Time: 10:30 To 01:30 Marks: 70

Instructions:

(1) Use of Programmable calculator & any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

Q-1 **Attempt the following questions:** **(14)**

a Digital number system is said to be of base or radix
(a)10 (b)2 (c) 0

b Binary code that distinguishes ten elements must contain at least
(a) Two bits (b) Three bits (c) Four bits (d) Five bits

c Code not included in code conversion standard is
(a) BCD code (b) gray code (c) excess3 code (d) truth table

d Gray to binary conversion can be implemented with
(a) AND (b) XOR (c) NAND (d) NOR

e 4bit gray code can be converted into
(a)4 bit binary (b) 3 bit binary (c) 2 bit binary (d) 1 bit binary

f Code conversion circuits mostly uses
(a)AND-OR gates (b)AND gates (c)OR gates (d)XOR gates

g A two valued Boolean algebra is defined as a set of
(a) three values (b) two values *(c)* four values *(d)* five values

h TTL digital logic family uses
(a) unipolar (b) bipolar

i (x*y)*z=x*(y*z) is the
(a)commutative property (b)inverse property (c)identity element (d)associative property

j Gray code representation of 14 is
(a)1010 (b)1100 (c) 1001

k Most significant bit of arithmetic addition is called
(a) overflow (b) carry (c) output (d) zero bit

l Two bit subtraction is done by
(a) demux (b) mux (c) full subtract (d) half subtract

m Basic building block digital circuit is/are

(a) NAND (b) NOR *(c)* AND *(d)* both a and b

n Exclusive-OR is an

(a) even function (b) odd function

Attempt any four questions from Q-2 to Q-8

Q-2 **Attempt all questions** **(14)**

A Draw the logic symbol and construct the truth table for all logic gates.

B Design and Implement a Half Adder

Q-3 **Attempt all questions** **(14)**

A Implement All basic gates using NAND and NOR logic.

B (i) Convert $(105.15)_{10}$ number into binary number.
(ii) Convert $(4057.06)_8$ into decimal number.
(iii) Convert $(10101)_2$ number into decimal number.
(iv) Convert $(4BAC)_{16}$ into binary.
(v) Convert $(756.603)_8$ into hex number.
(vi) Convert binary 1001 to gray code
(vii) Find 2's compliment of -45 in 8-bit form.

Q-4 **Attempt all questions** **(14)**

A (i) Implement the Boolean Expression in AOI logic.

$$Y= A+BC'+(B+C)'+B'C'$$

(ii)Reduce the Expression (B+BC) (B+B'C) (B+D)

B Obtain the minimal SOP expression for $\sum m(0,1,4,5,6,7,9,11,15) + d(10,14)$
And implement it in AIO logic

Q-5 **Attempt all questions** **(14)**

A Design and Implement a 4-bit Binary to Grey code converter.

B Design and Implement a 3-line to 8-line decoder.

Q-6 **Attempt all questions** **(14)**

A With neat sketch explain the operation of Edge Triggered J-K flip flop.

B Design and Implement a 1-line to 8-line demultiplexer.

Q-7 **Attempt all questions** **(14)**

A With neat diagram explain the operation of 4- bit parallel- in Serial-out Shift register.

B Comparison of Counters and Registers.

Q-8 **Attempt all questions** **(14)**

A Design and implement a synchronous 3-bit up counter using j-k flip flops.

B What are the applications of shift register?